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10/022,854	12/20/2001	Seung Kuk Ahn	049128-5030	1440

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EXAMINER	
LAO, LUN YI	

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2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/022,854	AHN, SEUNG KUK	
	Examiner	Art Unit	
	LUN-YI LAO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/5/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6* is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/6/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi(6,329,975) in view of Eto et al(5,301,031).

As to claims 1 and 3, Yamaguchi et al teach an LCD display comprising the steps of: receiving a data enable signal(DATA ENABLE SIGNAL) from interface circuit(computer) to a timing controller(4-9) for indicating a time interval when a video data exists(see figures 1-3; column 1, lines 10-15 and lines 54-68 and column 2, lines 1-13); detecting an enable initiation time of the data enable signal ; generating a reset signal(Hsp1 or Hsp2) at the enable initiation time of data signal(DATA ENABLE SIGNAL)(see figures 1-3; column 4, lines 42-55 and column 5, lines 9-37); resetting(adjust again) a source shift clock(8) in response to the reset signal(the source shift clock signal(Hsp) is generated again when the resetting signal(Hsp1 or Hsp2) is available)(see figures 1-2A), wherein the source shift clock(8) is reset at the enable

initiation time in response to the reset signal(see figures 2-4; column 1, lines 54-68 and column 2, lines 1-54).

As to claim 3, Yamaguchi et al teach a driving apparatus for a liquid crystal display comprising a source shift clock reset unit(11 or 7) for detecting an enable initiation time of a data enable signal from an interface circuit(computer) being input to a timing controller(4-9) for indicating a time interval when a video signal exists to generate a reset signal(Hsp1 or Hsp2); a reference clock generator(8) for generating a source shift clock at the enable initiation time(see figures 2-4; column 1, lines 54-68 and column 2, lines 1-54).

Yamaguchi fail to disclose a source shift clock for sampling the video signal.

Eto et al teach a source shift clock(7) for sampling the video signal(see figures 1-2; column 3, lines 1-50 and column 4, lines 4-12). It would have been obvious to have modified Yamaguchi with the teaching of Eto et al, so as to provide high display quality without using an external memory.

3. Claims 2 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi in view of Eto et al in view of Sekido et al(5,999,158).

Yamaguchi as modified fail to disclose a source driving circuit for latching video signal after sampling.

Sikido et al teach a source driving circuit having a latching circuit(4) for latching sampling video signal(see figure 4; column 3, lines 61-68 and column 4, lines 1-4). It would have been obvious to have modified Yamaguchi as modified with the teaching of

Sekido et al, so as to transfer sampling data signal to an LCD display panel(see column 4, lines 2-4).

4. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno(6,559,839) et al in view of Eto et al(5,301,031).

As to claims 1 and 3, Ueno et al teach an LCD display comprising the steps of: receiving a data enable signal(DENAB) from interface circuit(computer or 1-5) to a timing controller(6) for indicating a time interval when a video data exists(see figure 1; column 2, lines 55-68 and column 3, lines 1-10); detecting(e.g. 7) an enable initiation time of the data enable signal(DENAB); generating a reset signal at the enable initiation time of data signal(DENAB); resetting(adjust again after detecting the DENAB) a source shift clock(8) in response to the reset signal(generating from Counter(7)), wherein the source shift clock(8) is reset at the enable initiation time in response to the reset signal(see figures 1-2; column 3, lines 13-31; and column 5, lines 27-37).

As to claim 3, Ueno et al teach a driving apparatus for a liquid crystal display comprising a source shift clock reset unit(7) for detecting an enable initiation time of a data enable signal from an interface circuit(1-5) being input to a timing controller(6) for indicating a time interval when a video signal exists to generate a reset signal(see figure 4); a reference clock generator(8) for generating a source shift clock at the enable initiation time(see figures 1-2; column 3, lines 13-31; and column 5, lines 27-37).

Ueno et al fail to disclose a source shift clock for sampling the video signal.

Eto et al teach a source shift clock(7) for sampling the video signal(see figures 1-2; column 3, lines 1-50 and column 4, lines 4-12). It would have been obvious to have

modified Ueno et al with the teaching of Eto et al, so as to provide high display quality without using an external memory.

5. Claims 2 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno in view of Eto et al in view of Sekido et al(5,999,158).

Ueno et al as modified fail to disclose a source driving circuit for latching video signal after sampling.

Sikido et al teach a source driving circuit having a latching circuit(4) for latching sampling video signal(see figure 4; column 3, lines 61-68 and column 4, lines 1-4). It would have been obvious to have modified Ueno et al as modified with the teaching of Sekido et al, so as to transfer sampling data signal to an LCD display panel(see column 4, lines 2-4).

6. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoon et al(6,718,478) in view of Eto et al(5,301,031).

As to claims 1 and 3, Yoon et al teach an LCD display comprising the steps of: receiving a data enable signal(DE) from interface circuit(computer) to a timing controller(see figure 2) for indicating a time interval when a video data exists(see figure 2; column 1, lines 18-23 and column 3, lines 6-18); detecting(50) an enable initiation time of the data enable signal(DE); generating a reset signal(output from the AND2, start to generating a clock signal(STH) again) at the enable initiation time of data signal(DE); resetting(start again or set again) a source shift clock(8) in response to the reset signal, wherein the source shift clock(60) is reset at the enable initiation time in

response to the reset signal(see figures 2-3; column 3, lines 6-52; and column 4, lines 1-15).

As to claim 3, Yoon et al teach a driving apparatus for a liquid crystal display comprising a source shift clock reset unit(50) for detecting an enable initiation time of a data enable signal from an interface circuit(computer) being input to a timing controller(see figure 2) for indicating a time interval when a video signal exists to generate a reset signal(output from the AND2, start to generating a clock signal(STH) again); a reference clock generator(60) for generating a source shift clock at the enable initiation time(see figures 2-3; column 3, lines 6-52; and column 4, lines 1-15).

Yoon et al fail to disclose a source shift clock for sampling the video signal.

Eto et al teach a source shift clock(7) for sampling the video signal(see figures 1-2; column 3, lines 1-50 and column 4, lines 4-12). It would have been obvious to have modified Yoon et al with the teaching of Eto et al, so as to provide high display quality without using an external memory.

7. Claims 2 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoon et al in view of Eto et al in view of Sekido et al(5,999,158).

Yoon et al as modified fail to disclose a source driving circuit for latching video signal after sampling.

Sekido et al teach a source driving circuit having a latching circuit(4) for latching sampling video signal(see figure 4; column 3, lines 61-68 and column 4, lines 1-4). It would have been obvious to have modified Yoon et al as modified with the teaching of

Sekido et al, so as to transfer sampling data signal to an LCD display panel(see column 4, lines 2-4).

Allowable Subject Matter

8. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Applicants argue that Yamaguchi's selector circuit(8) is not a source shift clock on page 10. The examiner disagrees with that since the selector circuit(8) for generating a source shift clock signal to a source driver(3)(see figures 1-2B and column 2, lines 7-54).

Applicants argue that that Yamaguchi does not teach a data enable signal from an interface circuit being input to a timing clock controller on page 10. The examiner disagrees with that since a data enable signal(DATA ENABLE SIGNAL) from interface circuit(computer) to a timing controller(4-9)(see figures 1-3; column 1, lines 10-15 and lines 54-68 and column 2, lines 1-13);

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yeo(6,049,320) teaches an LCD display comprising a data driver having a data enable signal.

Shimada(6,512,506) teaches a timing generator for receiving a data enable signal.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi Lao whose telephone number is 571-272-7671. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 4, 2007

Lun-yi Lao
Primary Examiner